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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,409	04/14/2004	Burnell G. West	NPT-65.0405	8168

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,409	WEST ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a Non-Final Action in response to the instant U.S. Application filed April 14, 2004, which claims priority of the copending provisional patent application, 60/463,166, filed April 15, 2003.

Claims 1-23 are pending and presently under examination.

Drawings

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings included hand written notations and shaded areas, thus making the drawings non legible. Shaded areas must be removed from the drawings, especially the areas that also include legends. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Abstract

The abstract of the disclosure is objected to because of minor informalities.

The Examiner is suggesting the following amended Abstract:

"A test apparatus and method of testing, including means for sending a first test pattern to a device under test (DUT), where the first test pattern is part of a planned sequence of tests, and further including means for evaluating the test results received

from the DUT. The test results may include anomalous data indicative of a defect in the DUT. If so, a second test pattern that is not pad of the planned sequence of tests is selected. The second test pattern is selected based on a diagnosis of the anomalous data by the test apparatus". Correction is required. See MPEP § 608.01(b).

Specification

The disclosure is objected to because of the following informalities:

The specification should be updated to include the related Application Number: 10/824703, filed: 04/14/2004, Title: CONFIGURABLE TESTER WITH DIAGNOSTIC CAPABILITY. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Wohl et al. (US 6,950,974), filed: September 7, 2001.

Regarding independent Claims 1, 9, 17, Wohl discloses an apparatus and method of testing an integrated circuit, IC (DUT) 130, by applying multiple test patterns to the inputs of the circuit and monitoring its outputs to detect the occurrence of faults, Figure 2A, comprising:

Sending a first test pattern (step 302) to the device under test (DUT) 130, using a pseudorandom pattern generator (PRPG) circuit, which generates a bit sequence for each of the scan chains (131-136), Figures 1B, 2A and 3A-C.

Evaluating test results (step 305) received from the DUT in MISR-LFSR 150, where the test results are analyzed to determine if a fault is detected, corresponding to anomalous data indicative of a defect in the DUT;

Automatically selecting a second test pattern (step 303) that is not part of the planned sequence of tests in (step 302), wherein the second test pattern is selected based on detected faults the DUT. Referring to Figure 3B, which describes the step of adding patterns to the set (i.e. step 303), a new pattern can be started with no care bits set in step 311. In step 312, a new test for detecting a fault can be provided to the pattern, as indicated in Figure 3C.

Regarding Claims 2, 10, 18, Wohl discloses the anomalous data is saved and evaluated by the test apparatus, using a computer readable program code, which includes computer readable program code that computes multiple tests for each pattern, wherein each test detects a fault associated with an integrated circuit (IC) design, as well as computer readable program code that computes multiple patterns for each seed.

Regarding Claims 3-6, 11-14, 19-21, Wohl discloses a plurality of pins for receiving signals from the DUT through output scan pins (SO), and for capturing and storing the test results. Scan chain 131 includes an input scan pin (si1) and an output scan pin (so1). Scan chains 132-136 include corresponding scan pins si2/so2, si3/so3, si4/so4, si5/so5, and si6/so6, respectively.

Regarding Claims 7, 8, 15, 16, 22, 23, Wohl discloses second test pattern (step 303) is selected from a plurality of pre-computed test patterns, wherein the second test pattern is selected according to the pattern, as shown in Figure 3B, which describes the step of adding patterns to the set (i.e. step 303), then a new pattern can be started with no care bits set in step 311. In step 312, a new test for detecting a fault can be provided to the pattern, as indicated in Figure 3C.

Pertinent Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kobayashi et al. (US 5,646,948) issued: July 8, 1997, discloses an apparatus and method for testing a plurality of semiconductor memories (MUT1, MUT2, . . . MUTn), Figures 1-4, including sending a first test pattern (corresponding to address A0, Figure 4) to a device under test (MUT), using pattern generator 2, which outputs a first test pattern part of a planned sequence of tests, as shown in Figures 1-4. The pattern generator 2 generates an address AO and write enable signals WE1, WE2, . . . therefor. Evaluating test results, by comparing data read (RD) received from the MUT

with the expected data (ED) using (XOR gate 4X) comparator for outputting a compared result that represents a (PASS "0") when the read data matches with the expected data, and for outputting a compared result that represents a (FAIL "1") when the read data does not match with the expected data, where the test results (RD) comprising anomalous data corresponding to the failed condition (FAIL "1") indicating a defect in the MUT, (See, Summary of the Invention and Figure 3). Automatically selecting a second test pattern that is not part of the planned sequence of tests, which is selected based on a diagnosis of the failed condition (FAIL "1") in the MUT, see Summary of the Invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

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4/12/06

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Office Action: Non-Final Rejection